CLAIMS

1 - 14. Canceled.

15. (Previously Presented) A method for controlling a switchmode power supply comprising:

generating a time-length signal that includes a first portion and a second portion that indicate a pulse duration of an output signal;

transmitting the first portion of said time-length signal to a counting means, and the second portion of said time-length signal to a selection means;

counting to a number based on said first portion of said time-length signal received by said counting means;

outputting a coarse adjusted signal from said counting means after counting to said predetermined number;

selecting a delay from a delay means based on said second portion of said time-length signal received by said selection means;

delaying said coarse adjusted signal a predetermined length of time based on said selected delay in said delay means; and

outputting the output signal after said predetermined delay.

16-63. Canceled.

64. (Previously Presented) A method for controlling a switchmode power supply in a plasma chamber comprising:

generating a time-length signal that includes a first portion and a second portion that indicate a pulse duration of an output signal;

transmitting the first portion of said time-length signal to a counting circuit, and the second portion of said time-length signal to a selection circuit;

counting to a number based on said first portion of said time-length signal received by said counting circuit;

outputting a coarse adjusted signal from said counting circuit after counting to said predetermined number;

selecting a delay from a delay circuit based on said second portion of said time-length signal received by said selection circuit;

delaying said coarse adjusted signal a predetermined length of time based on said selected delay in said delay circuit; and

outputting the output signal to said power supply in said plasma chamber after said predetermined delay.

65. (Previously Presented) The method of claim 64, wherein said counting circuit is a digital circuit.

66. (Previously Presented) The method of claim 65, wherein said digital counting circuit comprises a programmable logic device.

67. (Previously Presented) The method of claim 66, wherein said counting circuit comprises an oscillator means operating at a predetermined frequency.

68. (Previously Presented) The method of claim 67, wherein said oscillator oscillates at approximately 125 MHz.

69. (Previously Presented) The method of claim 64, wherein said delay circuit delays in increments of 0.25 nanoseconds.

70. (Previously Presented) The method of claim 64, wherein said delay circuit is an analog circuit.

71. (Previously Presented) The method of claim 64, wherein said delay circuit is a digital circuit.

72. (Previously Presented) The method of claim 70, wherein said delay circuit comprises a plurality of inductors and capacitors connected in a series-parallel configuration.

73. (Previously Presented) The method of claim 64, wherein said selection circuit is a digital selection circuit.

74. (Previously Presented) The method of claim 64, wherein said selection circuit is a multiplexor.

75. (Previously Presented) The method of claim 64, wherein said processor operates at a first voltage, and said counting circuit, delay circuit, and selection circuit operates at a second voltage.

76. (Previously Presented) The method of claim 75, wherein said apparatus further comprises a first and second transform circuit, a power converter, and a power conditioner, wherein an output of said processor is coupled to said first transform circuit for transforming said output of said processor at said first voltage to said second voltage, and an output of said second selection circuit is coupled to said power converter, said second transformer means is coupled to said power converting means, said second transform circuit, and said power conditioner.

77. (Previously Presented) The method of claim 64, wherein said counting circuit, said delay circuit and said selection circuit is disposed in said processor.

78. (Previously Presented) The method of claim 64, wherein the step of generating a time-length signal further comprises generating said time-length signal in a processor.

79. (Previously Presented) The method of claim 64, wherein said counting circuit is a digital circuit.